Task 0

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| S1 | S2 | A | B | C | D | E | F |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

|  |  |  |
| --- | --- | --- |
| S1 | S2 | A |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

A =

S1 A

|  |  |  |
| --- | --- | --- |
| S1 | S2 | B |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

B =

S1

B

S2

|  |  |  |
| --- | --- | --- |
| S1 | S2 | C |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

C =

S1

C

S2

|  |  |  |
| --- | --- | --- |
| S1 | S2 | D |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

D = S1.S2

S1

D

S2

|  |  |  |
| --- | --- | --- |
| S1 | S2 | E |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

E = S1 + S2

E

S1

S2

|  |  |  |
| --- | --- | --- |
| S1 | S2 | F |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

F = S1 S2

S1

F

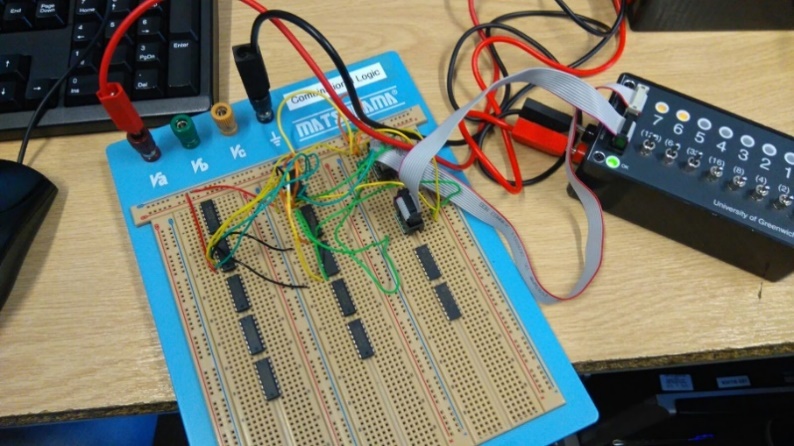
S2

Task 1

Demonstrate the circuit's operation to the tutor, and upload to your logbook, the truth table, a description of the function of the circuit, clearly **indicating the purpose the inputs and outputs.   
A circuit diagram of the three of the circuits connected together with the function of all inputs and** outputs clearly marked - **state where any unused input or outputs would be connected to within a computer**. Give three examples showing the circuit's operation.

Physical:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S7 | S6 | S5 | L7 | L6 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |



Figure

One member of the team constructed the circuit and Figure 1 shows how this was made. Figure 2 and 3 shows different results from the circuit made.

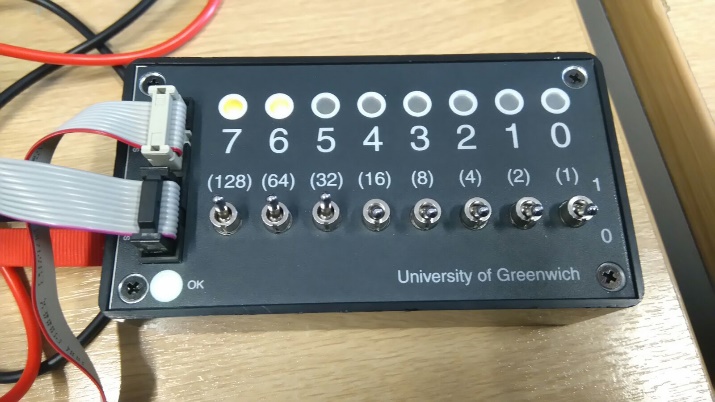
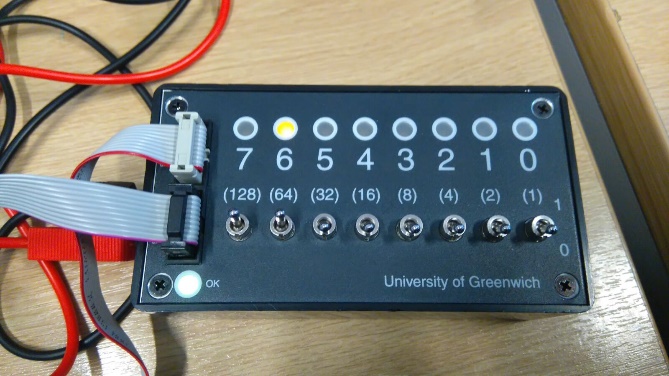
Calculation:

Figure – Results from constructed circuit

Figure – Results from constructed circuit

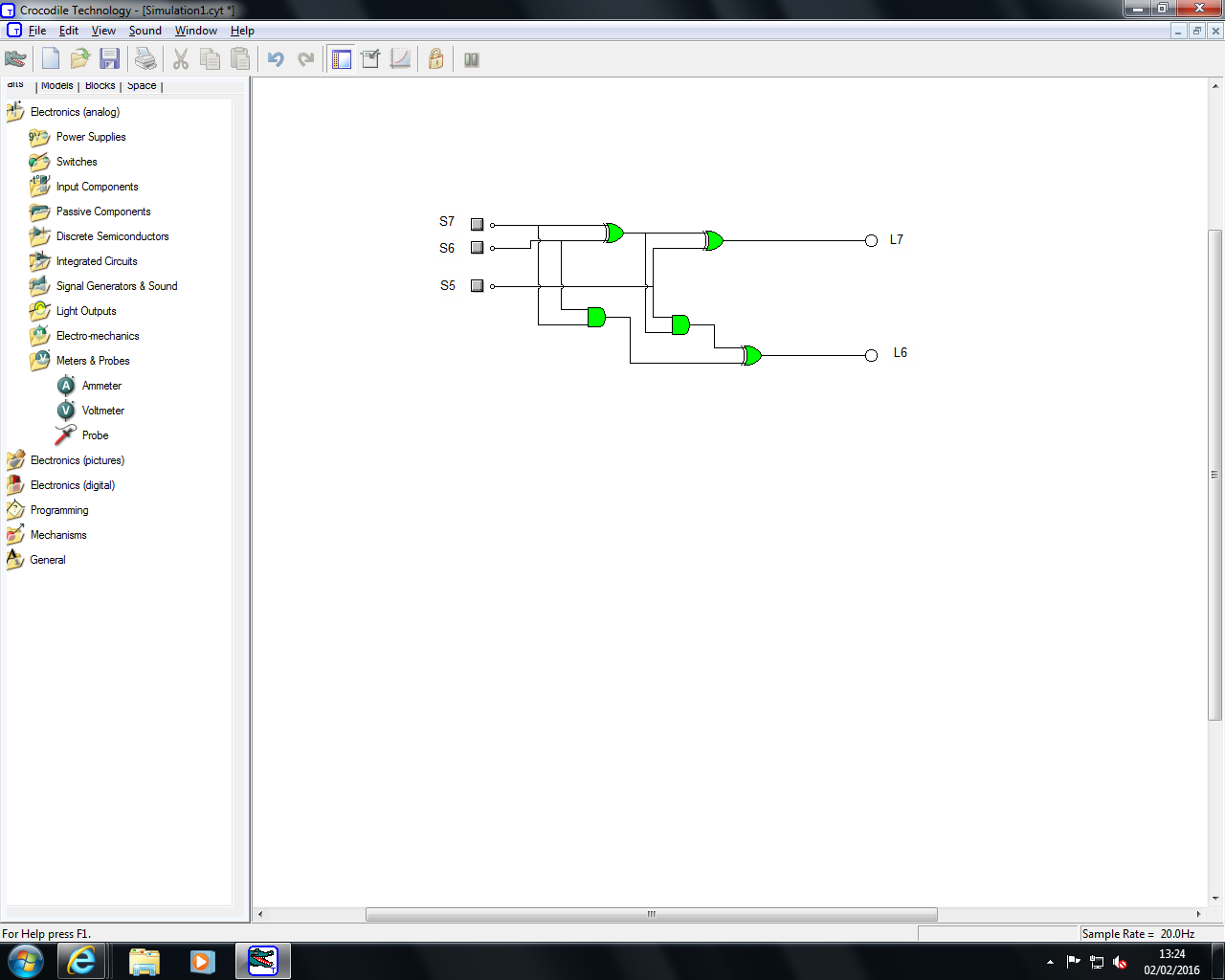
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S7 | S6 | S5 | L7 | L6 |
| 0 | 0 | 0 | **0** | **0** |
| 0 | 0 | 1 | **1** | **0** |
| 0 | 1 | 0 | **1** | **0** |
| 0 | 1 | 1 | **0** | **1** |
| 1 | 0 | 0 | **1** | **0** |
| 1 | 0 | 1 | **0** | **1** |
| 1 | 1 | 0 | **0** | **1** |
| 1 | 1 | 1 | **1** | **1** |

This was calculated by one member of the team and the results are shown.

|  |  |
| --- | --- |
|  |  |

Software:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S7 | S6 | S5 | L7 | L6 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |



This was used on Crocodile Clip software where we the truth table shows the results of the circuit made on the software.

Task 2  
Demonstrate the circuit's operation to the tutor and upload to your logbook, the truth table, the Karnaugh map and the circuit diagram.

Truth Table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| J | M | S |  | J.M | M. | M+S |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |

The Karnaugh map Circuit Diagram

|  |  |  |
| --- | --- | --- |
| J/M | 1 | 0 |
| 1 | 1 | 0 |
| 0 | 0 | 0 |

J

M

J.M

|  |  |  |
| --- | --- | --- |
| M/ | 1 | 0 |
| 1 | 1 | 0 |
| 0 | 0 | 0 |

S

S

M

|  |  |  |
| --- | --- | --- |
| M/S | 1 | 0 |
| 1 | 1 | 1 |
| 0 | 1 | 0 |

M

M + S

S

Task 3  
Construct the Karnaugh map for the segment controlled by 'bit 5' and implement the circuit.  Connect the switch light box and the dual seven segment display to the breadboard and demonstrate the circuit's operation to the tutor. Upload the Karnaugh map and circuit diagram to your logbook

Truth Table

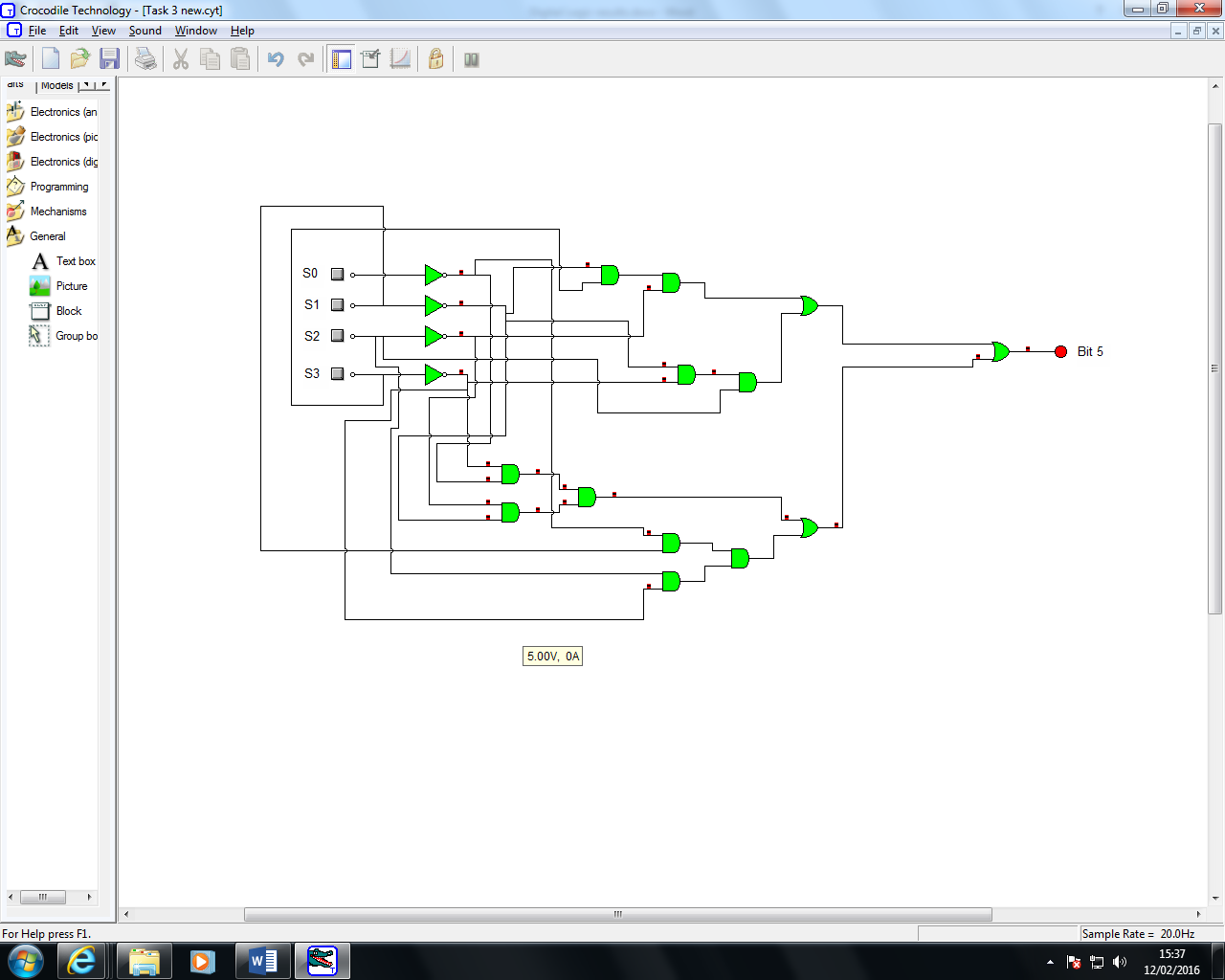
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S3 | S2 | S1 | S0 | Bit 5 |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |

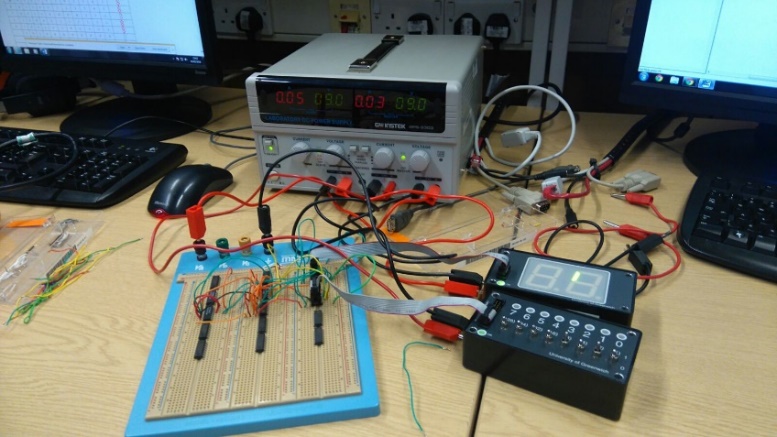
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S3 S2\S1 S0 | 00 | 01 | 11 | 10 |
| 00 | 1 | 0 | 0 | 0 |
| 01 | 1 | 1 | 0 | 1 |
| 11 | 0 | 0 | 0 | 0 |
| 10 | 1 | 1 | 0 | 0 |

Karnaugh Map

Boolean Equation:-

(. S3. ) + (. . . ) + (..S2) + (.S2.S1.)

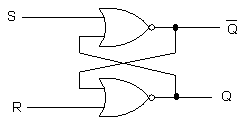
Circuit Diagram

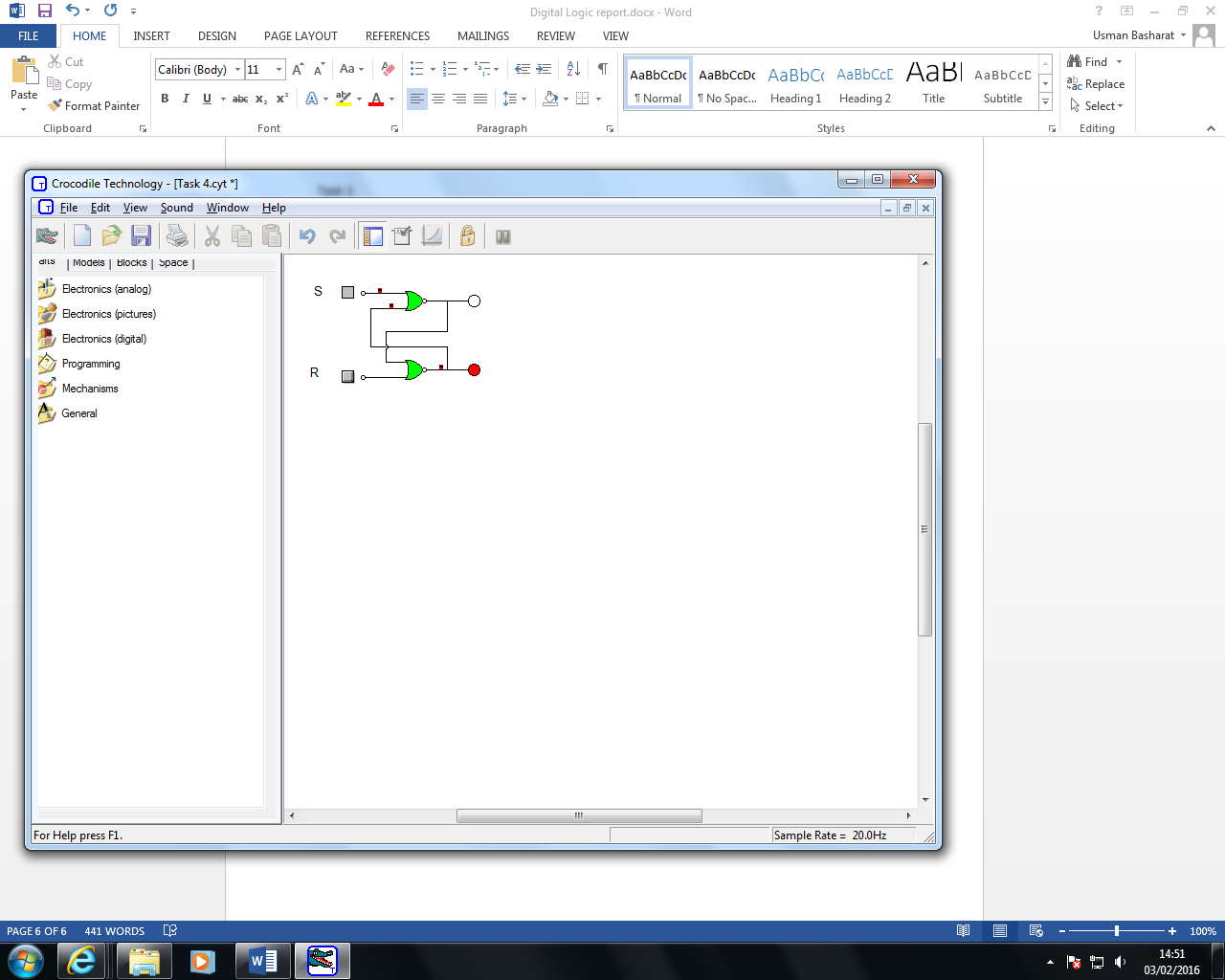


Figure

Task 4

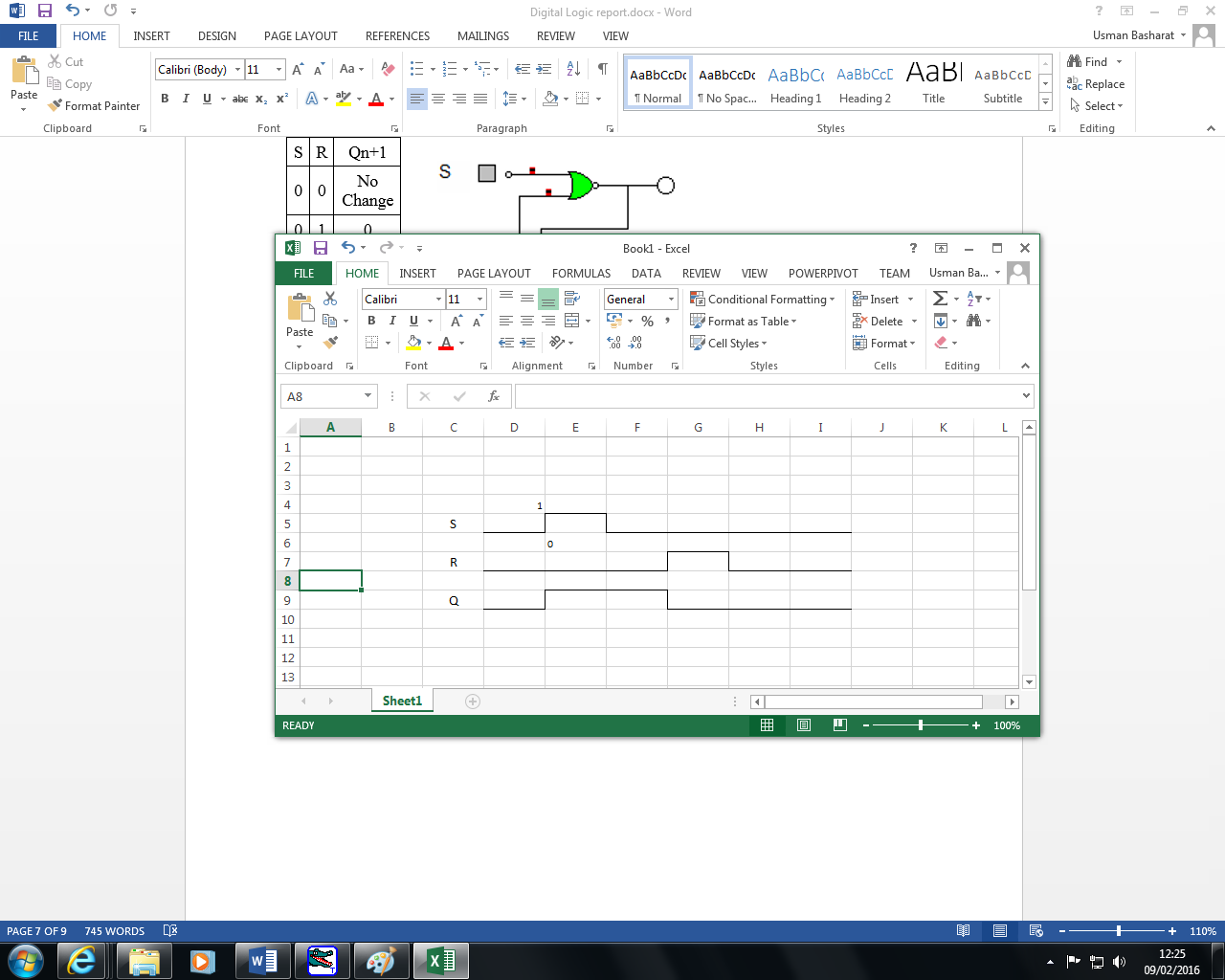
|  |  |  |
| --- | --- | --- |
| S | R | Qn+1 |
| 0 | 0 | No Change |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | Forbidden |

  
  
Upload to your logbook, the truth table and timing diagrams. State the purpose of the circuit.

Truth Table for Crocodile Clip

|  |  |  |
| --- | --- | --- |
| S | R | Qn+1 |
| 0 | 0 | No Change |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | Forbidden |

Timing Diagram

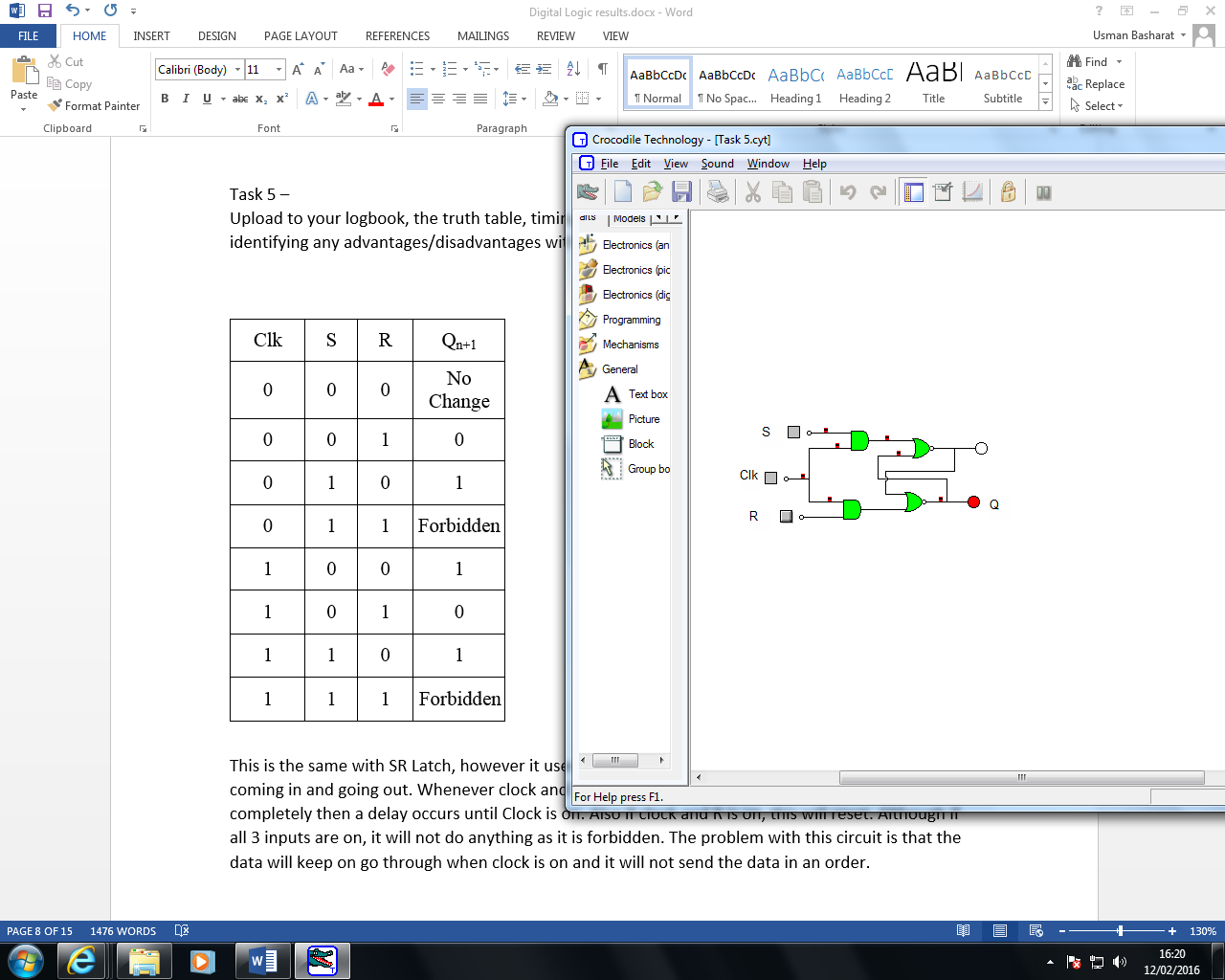


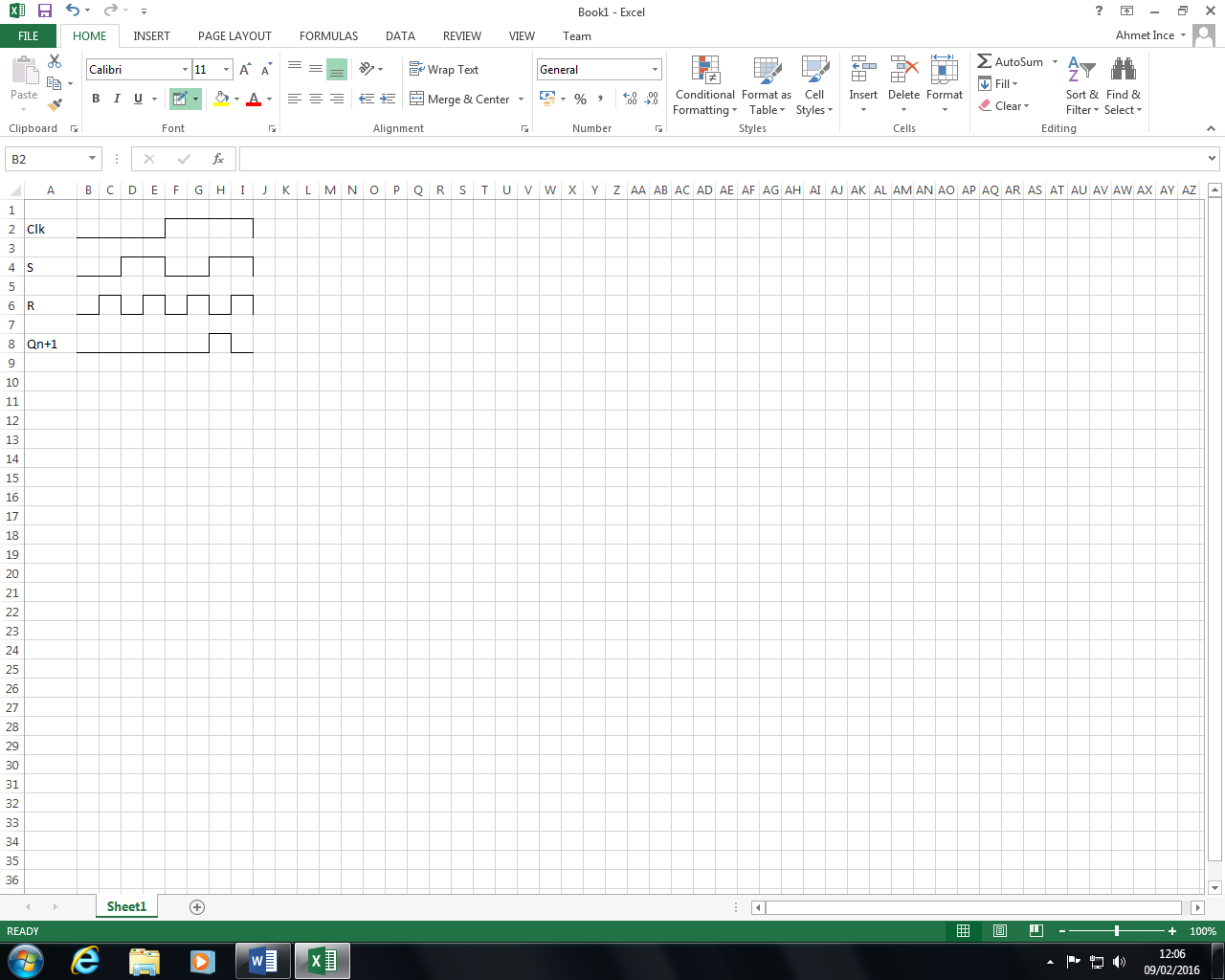
**State purpose of the circuit**

The purpose of this circuit this circuit that is an asynchronous device that works independently by relying on the two inputs Set and Reset. This is why both of them cannot work together. They need to rely on one or other for the circuit to work.

Task 5  
Upload to your logbook, the truth table, timing diagram and discuss the function of the clock, identifying any advantages/disadvantages with respect to the SR latch.

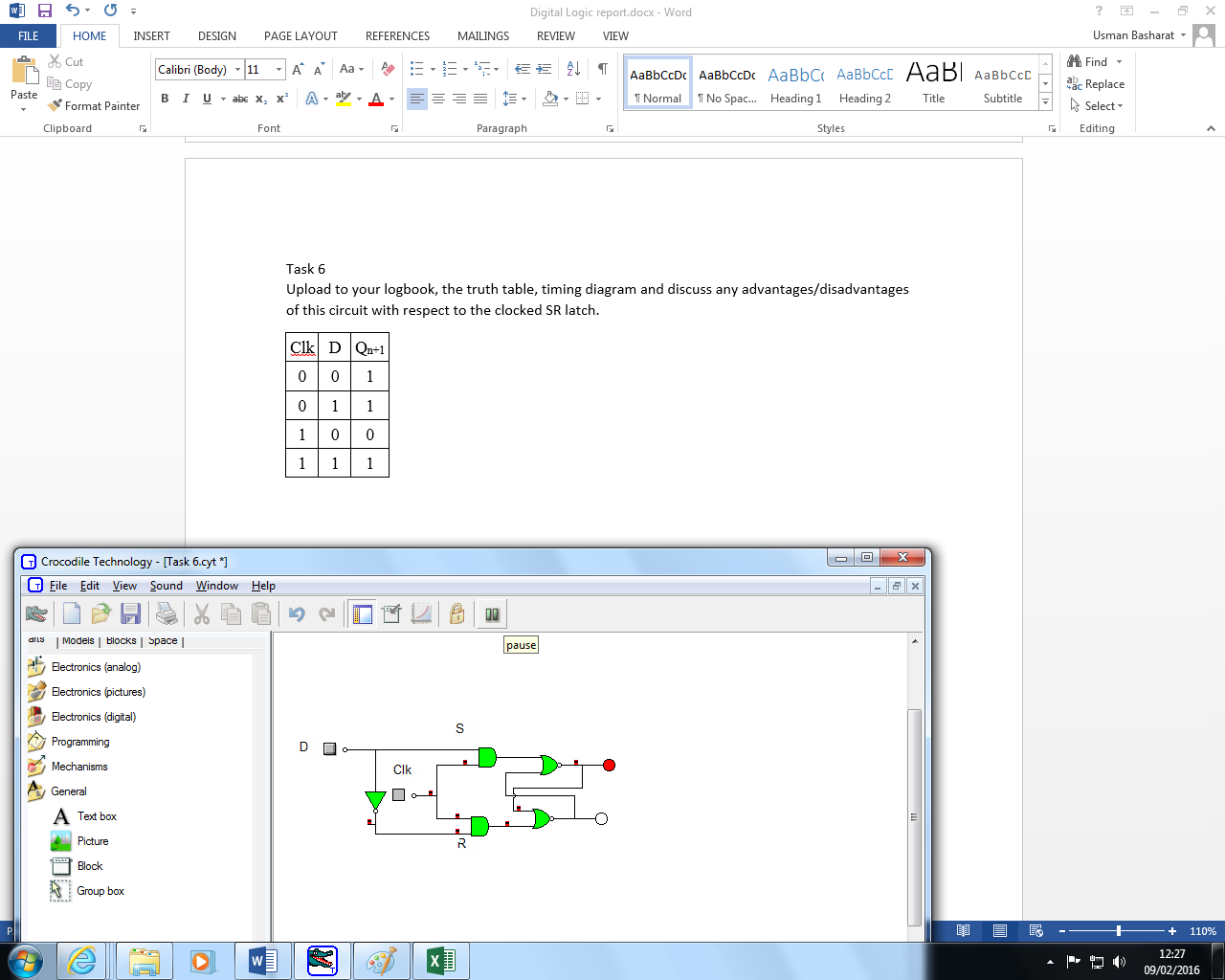
|  |  |  |  |
| --- | --- | --- | --- |
| Clk | S | R | Qn+1 |
| 0 | 0 | 0 | No Change |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | Forbidden |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | Forbidden |

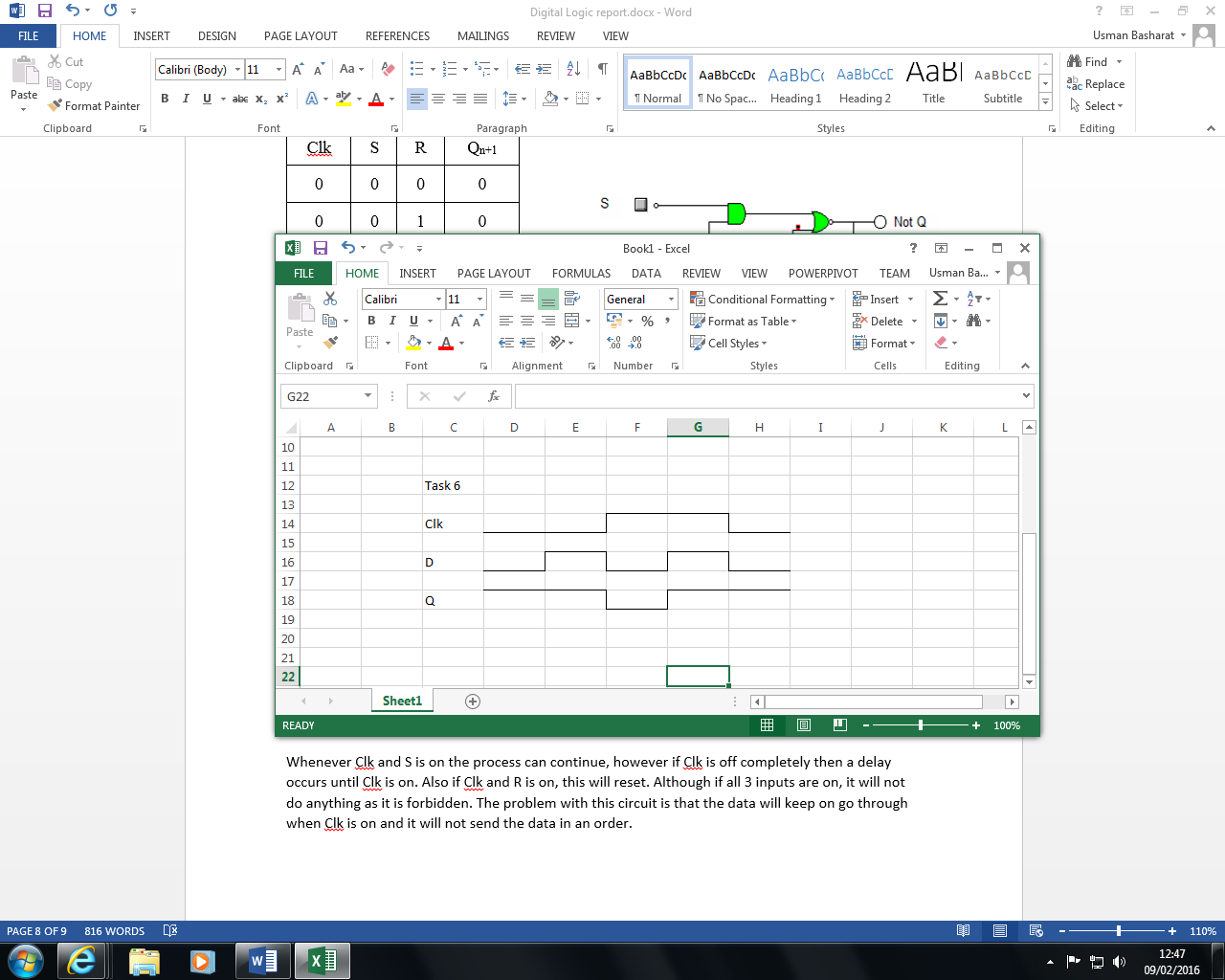




This is the same with SR Latch, however it uses a clock. The purpose of the clock is to time what is coming in and going out. Whenever clock and S is on the process can continue, however if clock is off completely then a delay occurs until Clock is on. Also if clock and R is on, this will reset. Although if all 3 inputs are on, it will not do anything as it is forbidden. The problem with this circuit is that the data will keep on go through when clock is on and it will not send the data in an order.

|  |  |  |
| --- | --- | --- |
| Clk | D | Qn+1 |
| 0 | 0 | No Change |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | Storing State |

Task 6  
Upload to your logbook, the truth table, timing diagram and discuss any advantages/disadvantages of this circuit with respect to the clocked SR latch.



**Advantage**

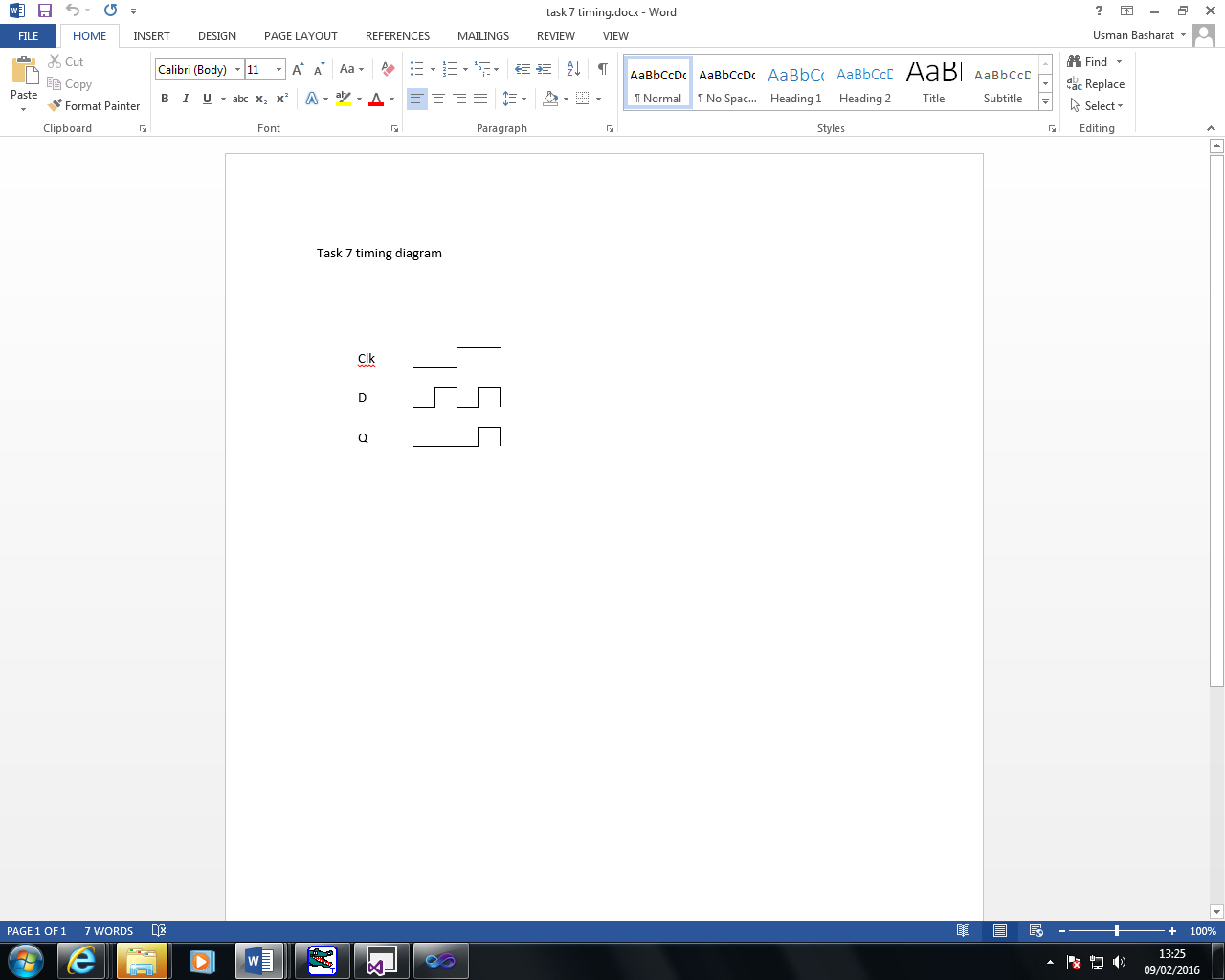
**Disadvantage**

Task 7

Upload to your logbook, the truth table and timing diagram. Apart from the preset and clear option on this device, state how this device's behaviour differs from the clocked D Latch above. With the aid of timing diagrams, discuss any advantages/disadvantage between the two.

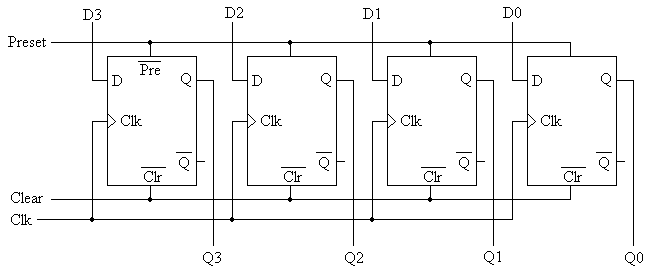
|  |  |  |
| --- | --- | --- |
| Clk | D | Qn+1 |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

1. D-latch is a level Triggering device while D Flip Flop is an Edge triggering device.  
        2. The disadvantage of the D FF is its circuit size, which is about twice as large as that of a D latch. That's why, delay and power consumption in Flip flop is more as compared to D latch.   
        3. Latches are used as temporary buffers whereas flip flops are used as registers.



Task 8

Construct the circuit below and establish it functionality.



This circuit is employed and works within the CPU. This is a 4 bit registers that has four outputs with 4 inputs coming from each of the register. These registers stores temporary memory. Therefore, for it to be 4 bit, the limited capacity storage of the temporary memory will be up to 4. There are extensive lengths, but this circuits shows this.

It uses storage forms such as registers and memory. The flip flop depends on both input and output for it to work. Flip flops are connected parallel and they are opposite to a latch.

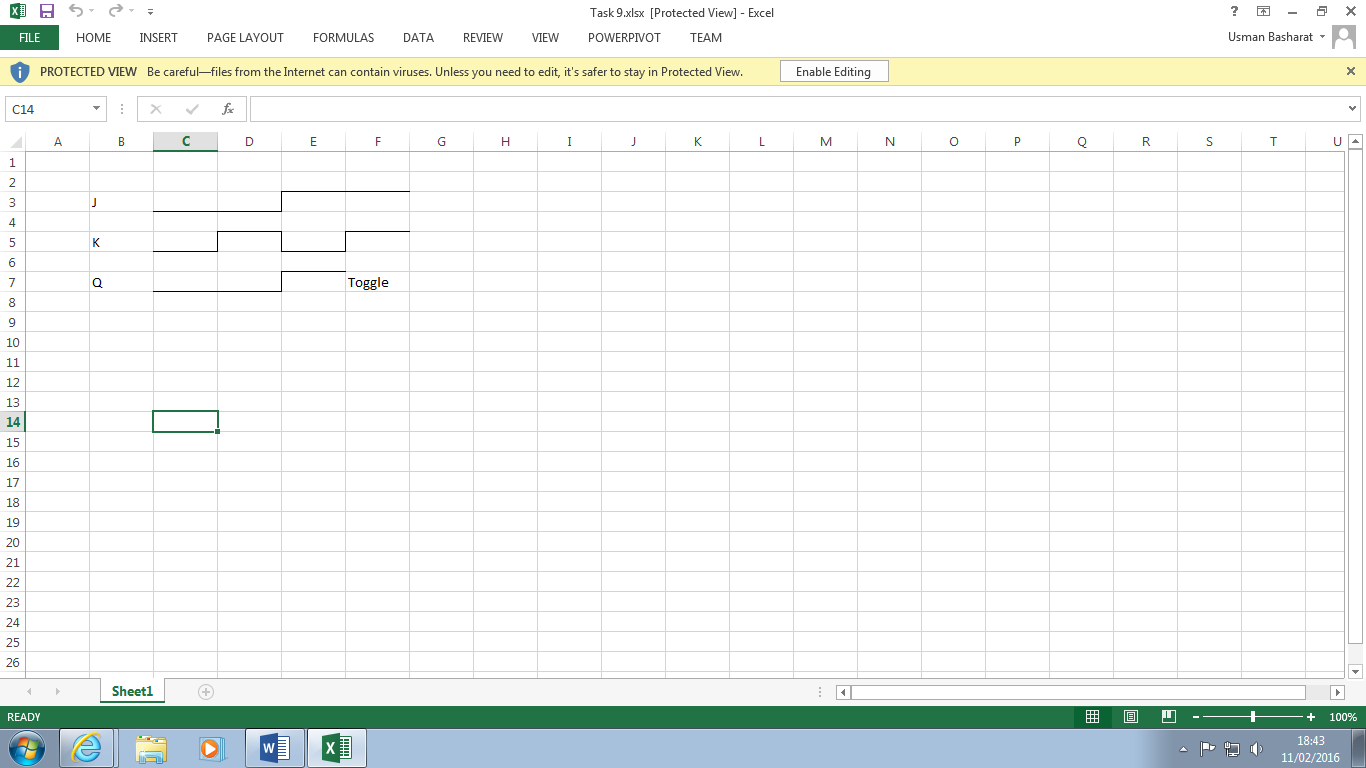
Task 9

Upload the truth table, timing diagram. With relation to the master slave arrangement of the circuit discuss the circuit's operation. Discuss where this circuit could be employed within a computer.



Figure

Timing Diagram



Truth Table

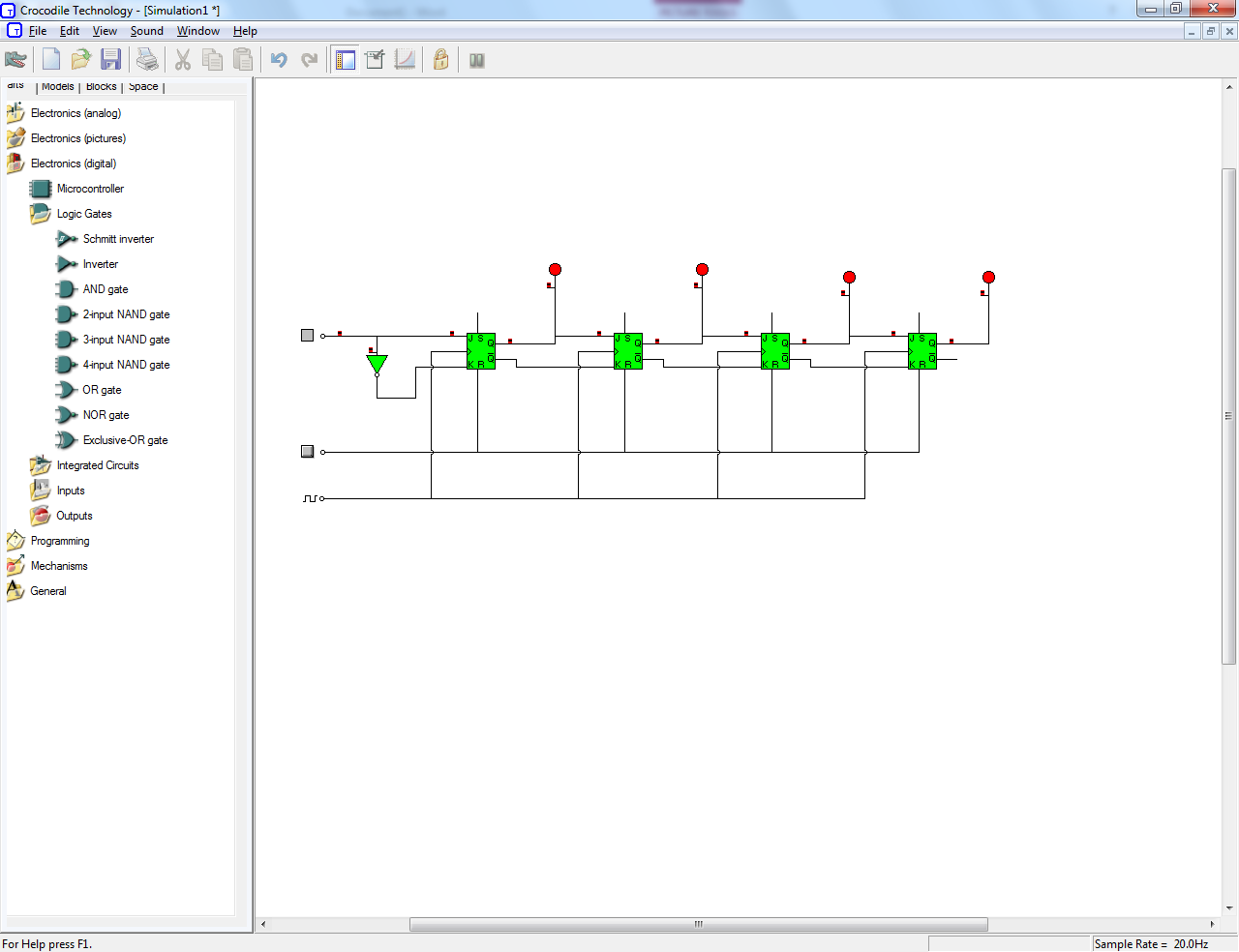
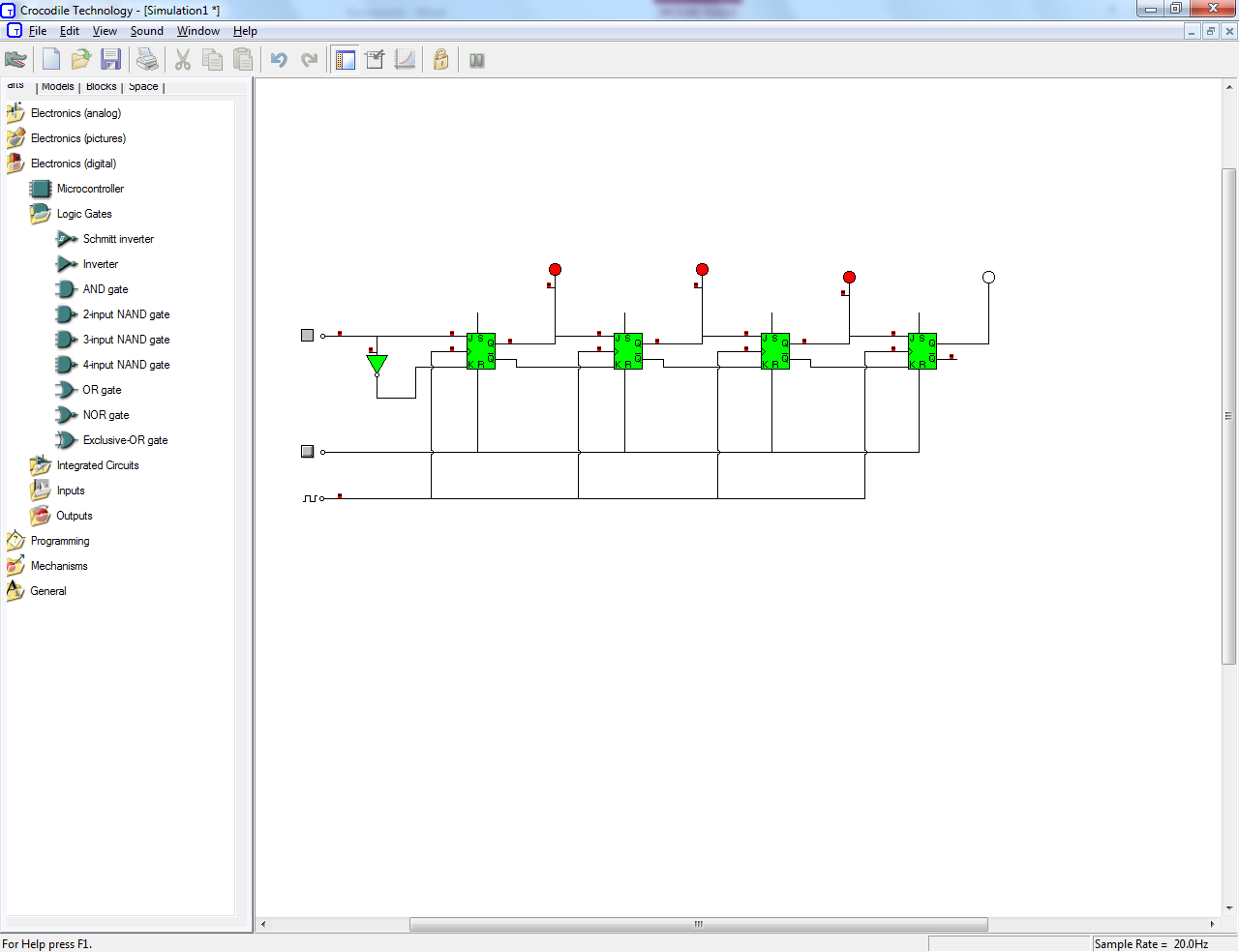
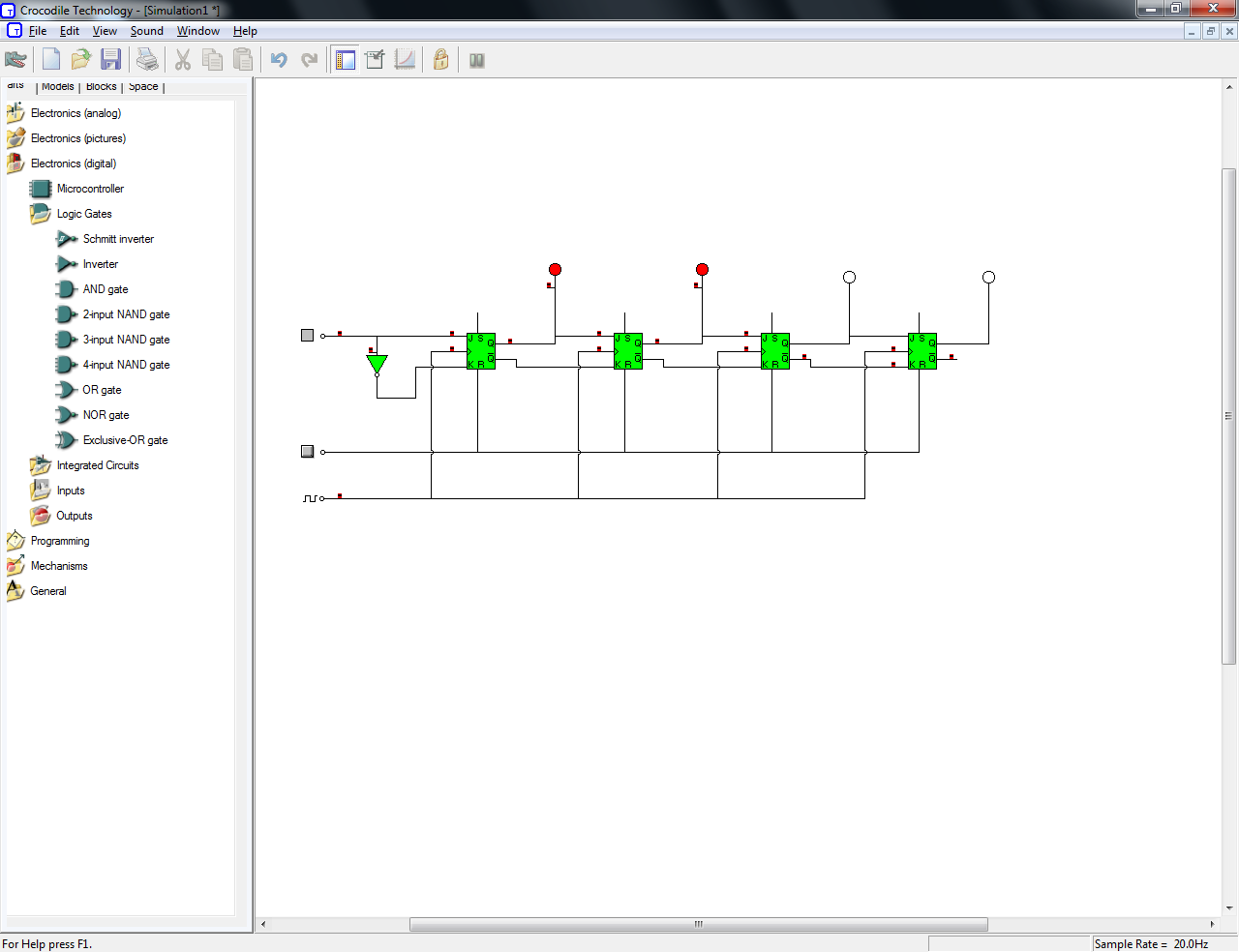
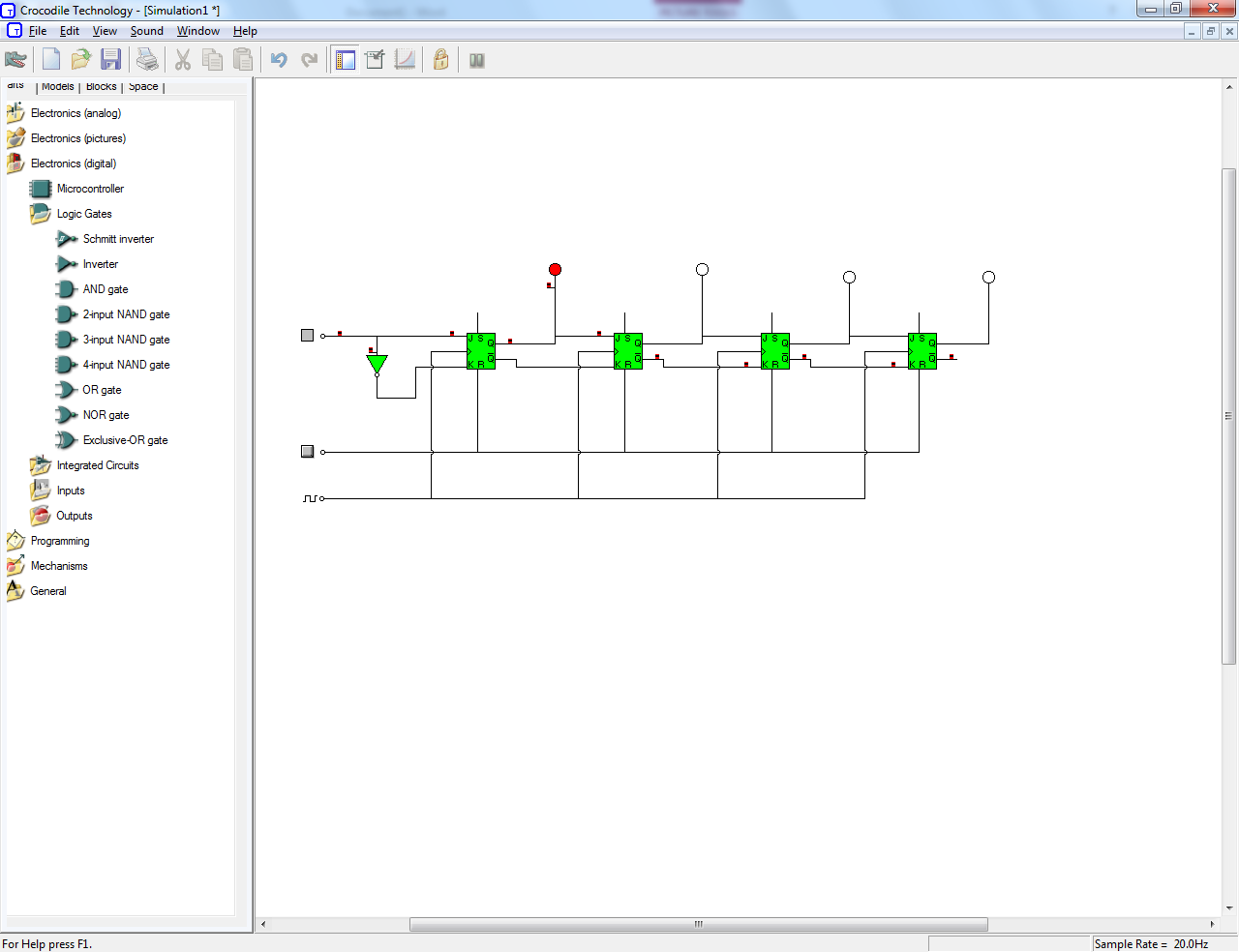
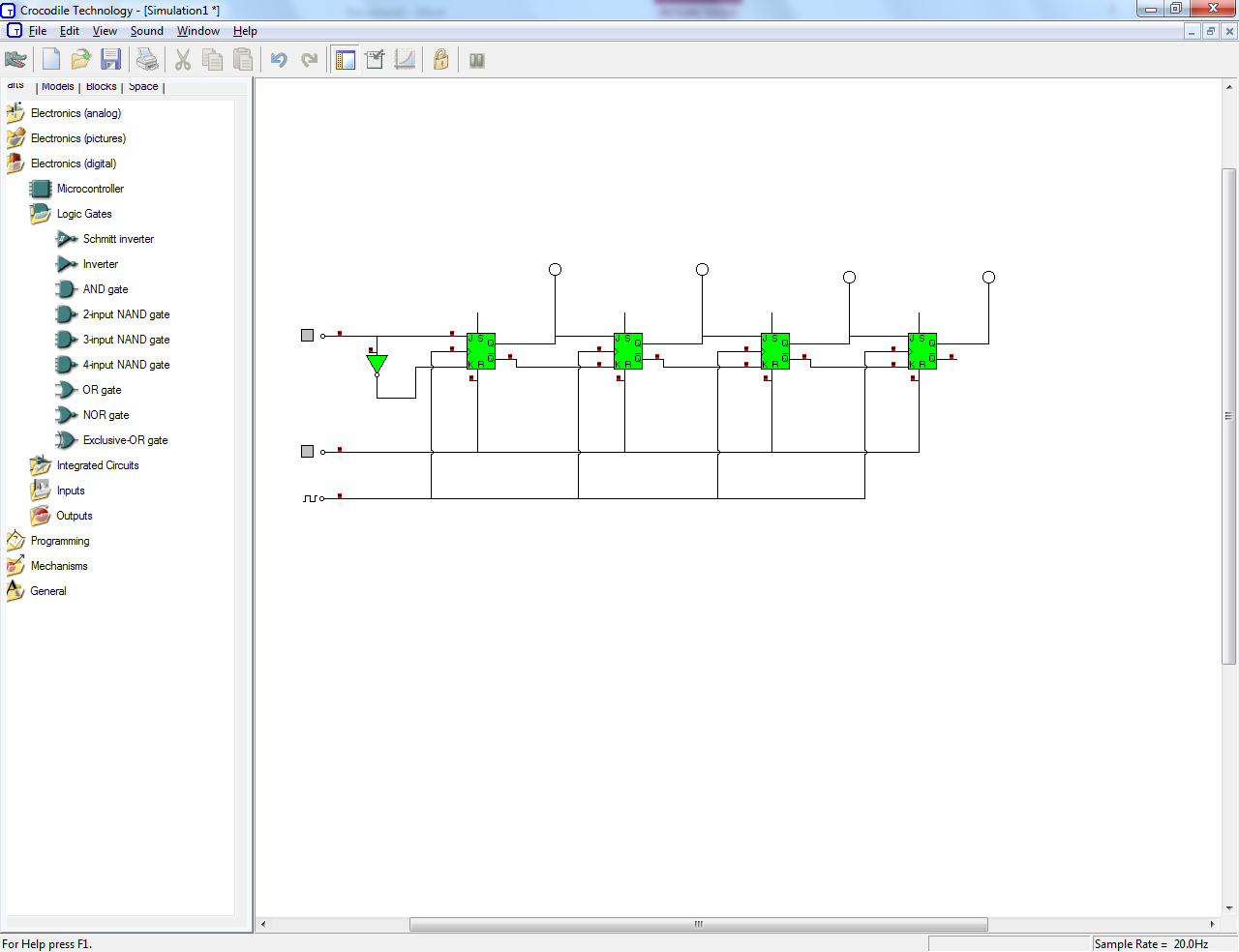
|  |  |  |
| --- | --- | --- |
| J | K | Qn+1 |
| 0 | 0 | No Change |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | Toggle |

Discuss where this circuit could be employed

This circuit can be used as memory in a computer.

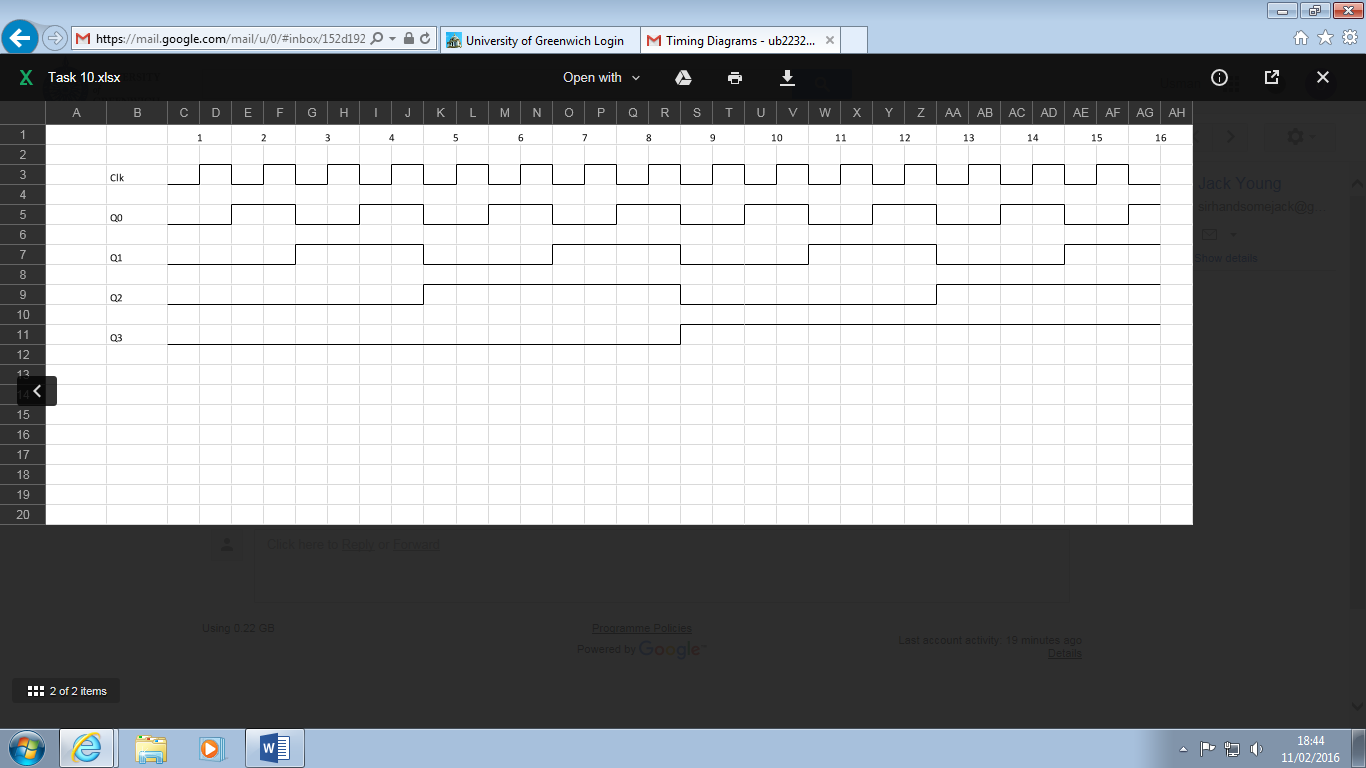
Task 10

What functions could this circuit perform? **Discuss how this circuit could perform division by 2.**

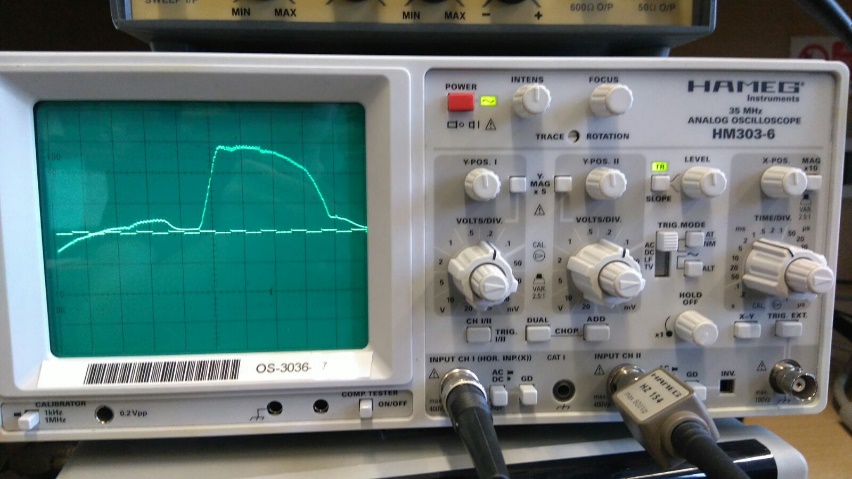


Shift register could be used as a circuit delay or as a converter from serial data to parallel data. Division by 2 can be done by shifting right one space and discarding the bottom bit. Shift registers are used as part of the CPU and ALU.

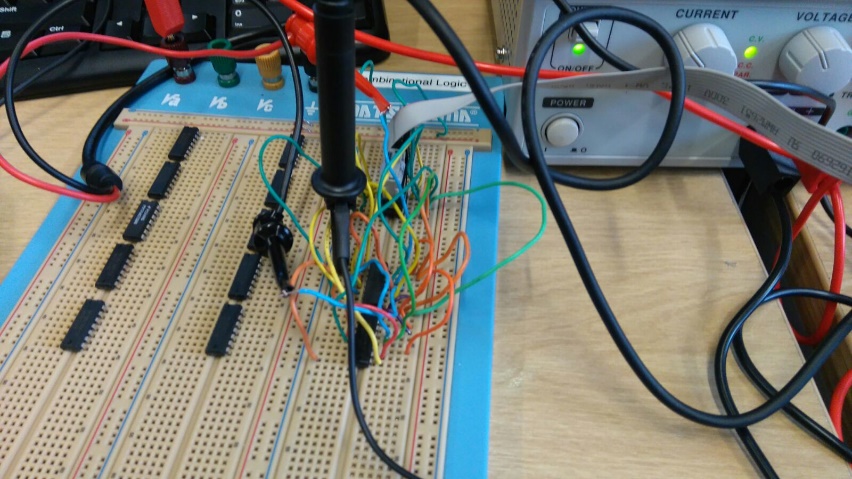
Task 11  
Upload the timing diagram showing the relative relationship of the waveforms at Clk, Q0, Q1, Q2 and Q3 Discuss where this circuit could be employed within a computer



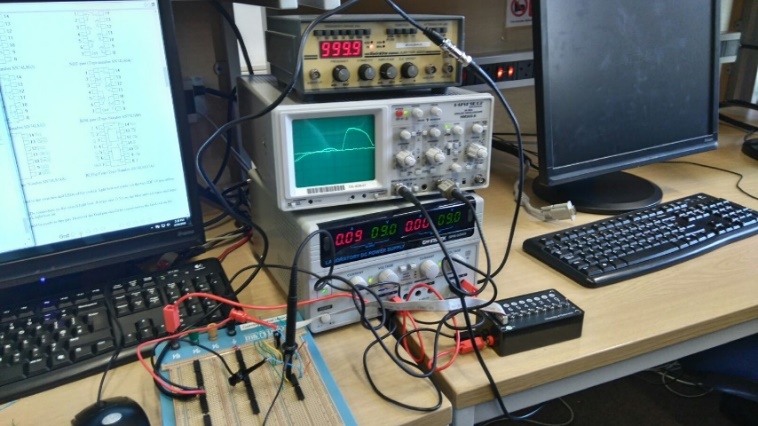
The circuit can be used as a program counter in the CPU of a computer.



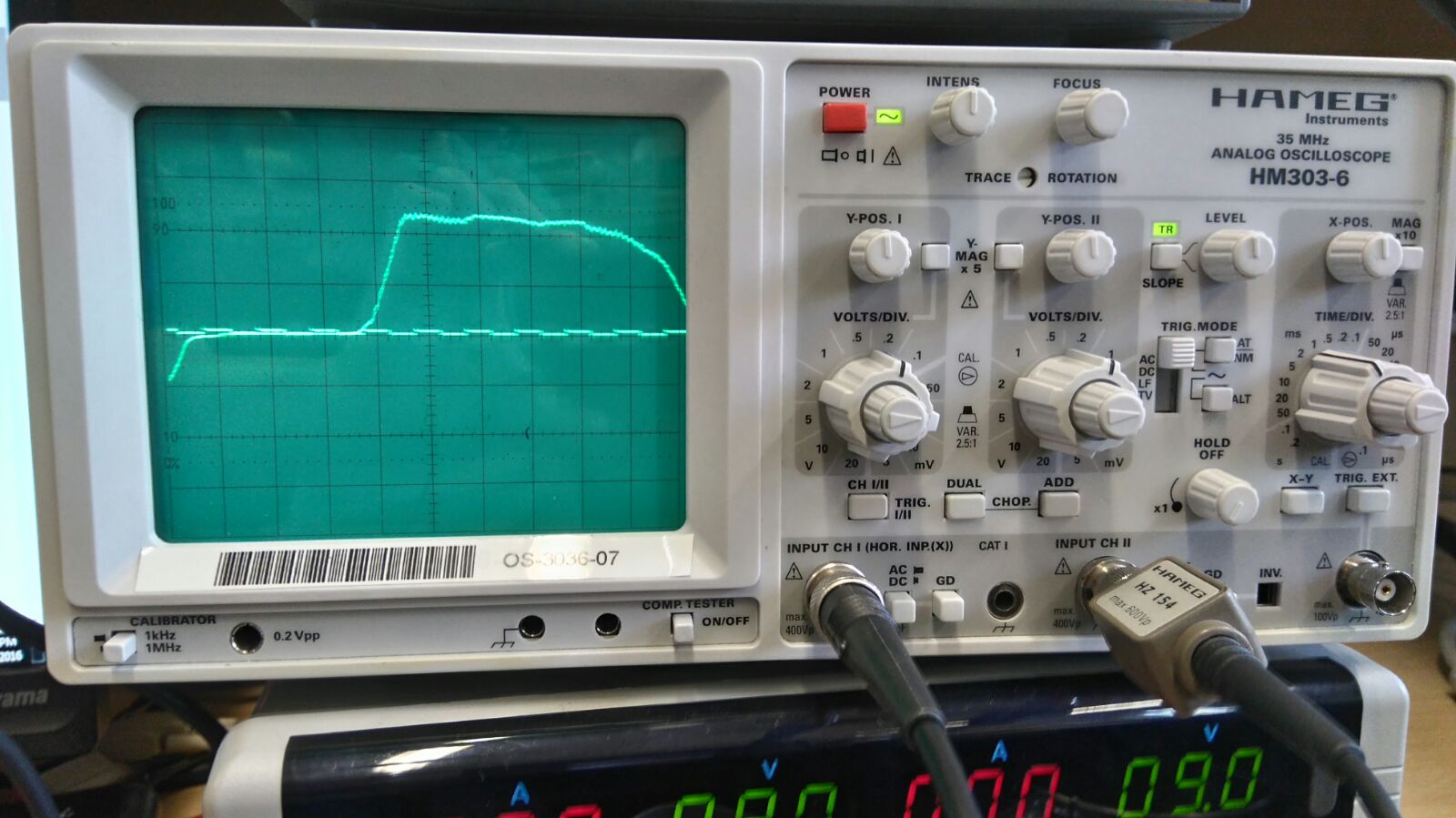
Figure



Figure

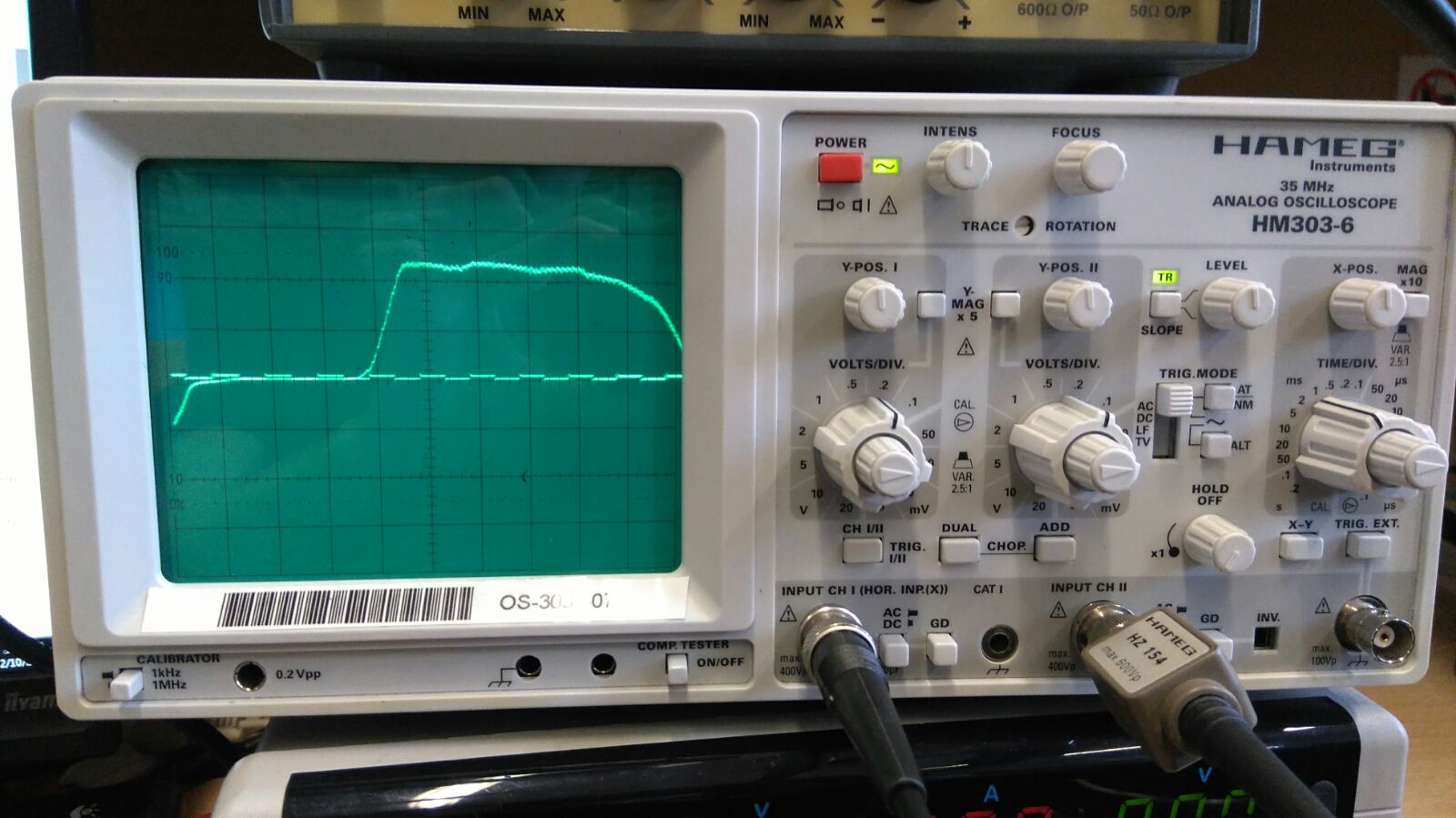


Figure



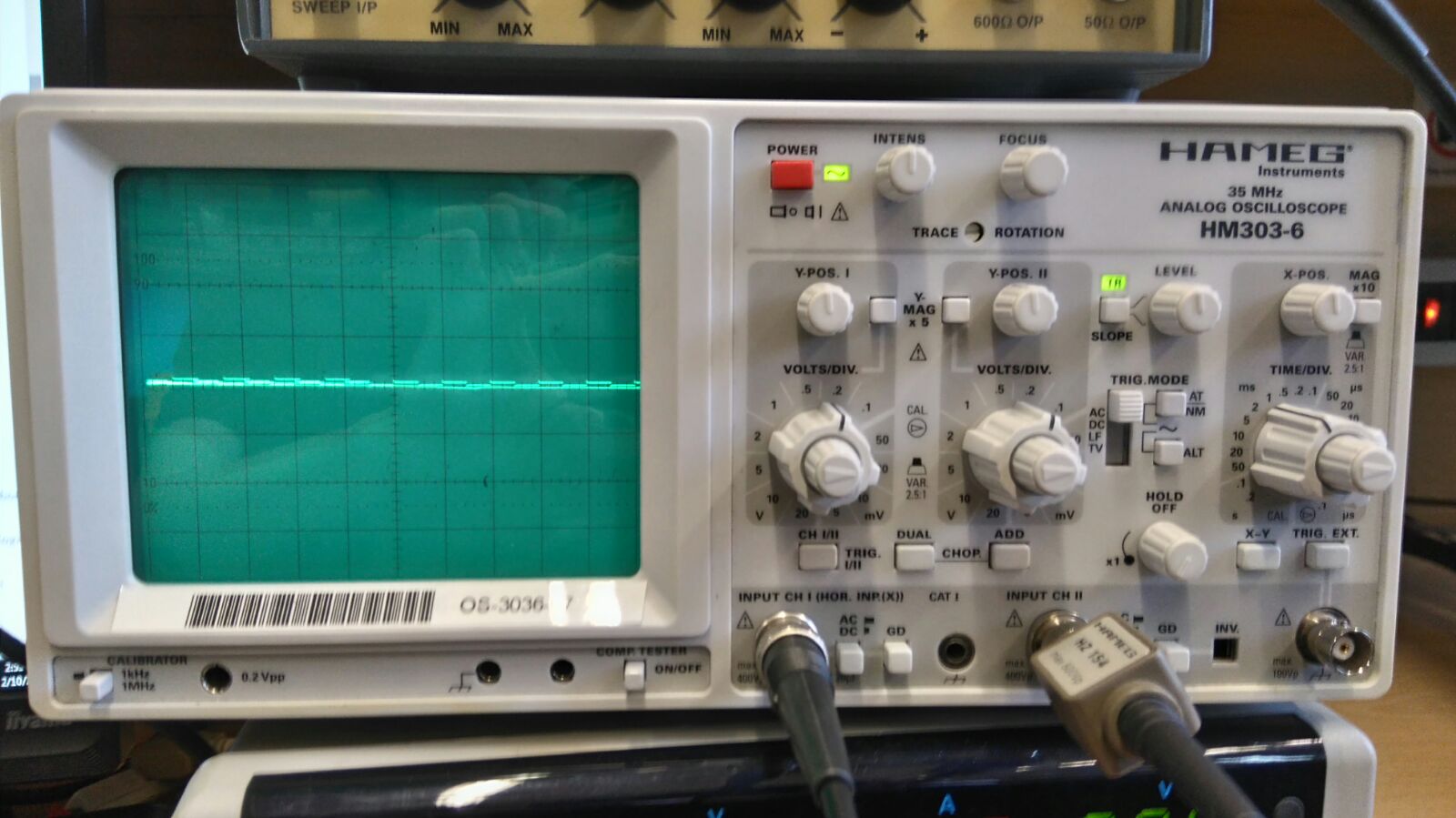
Figure

Q0



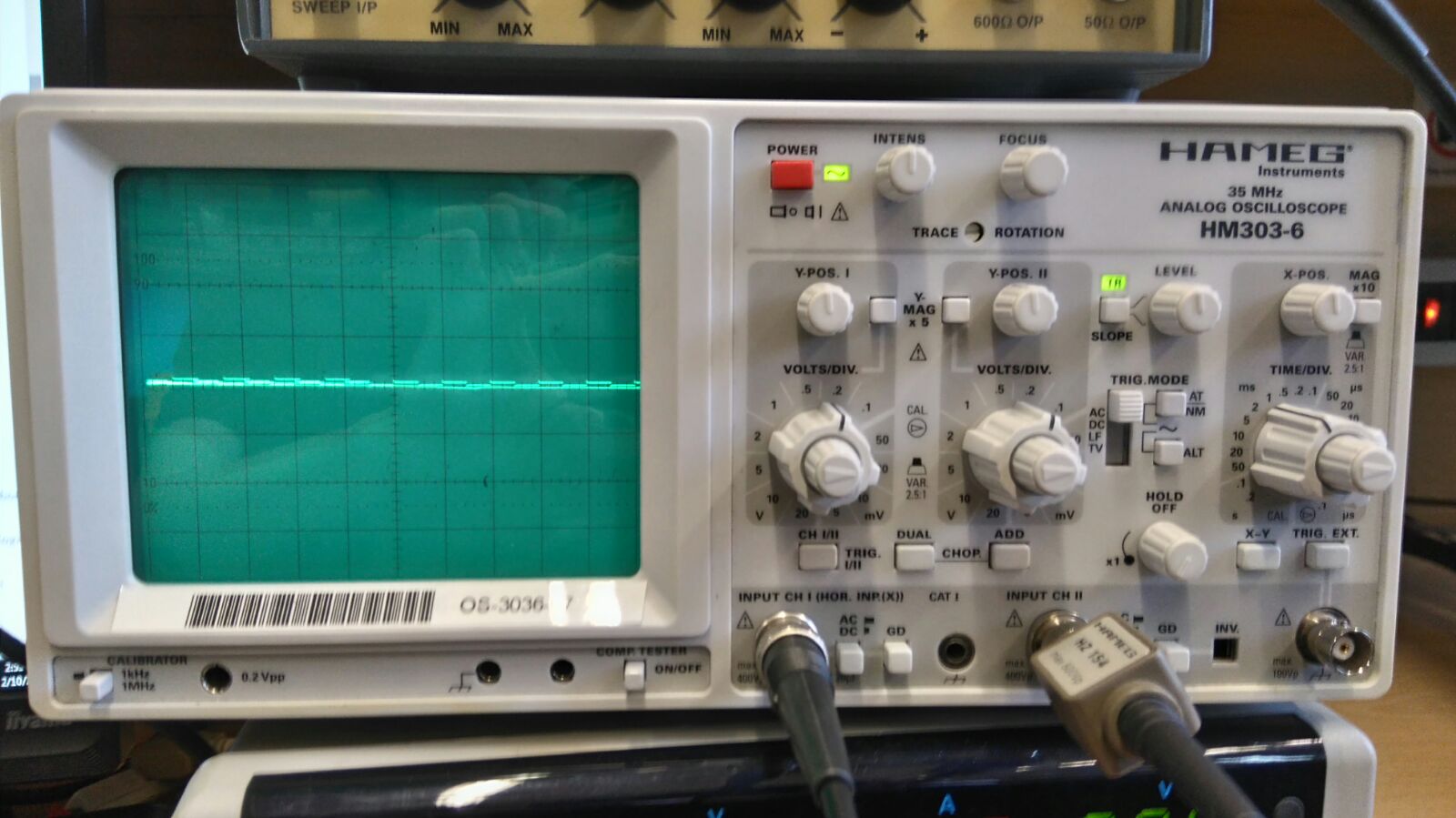
Figure

Q1



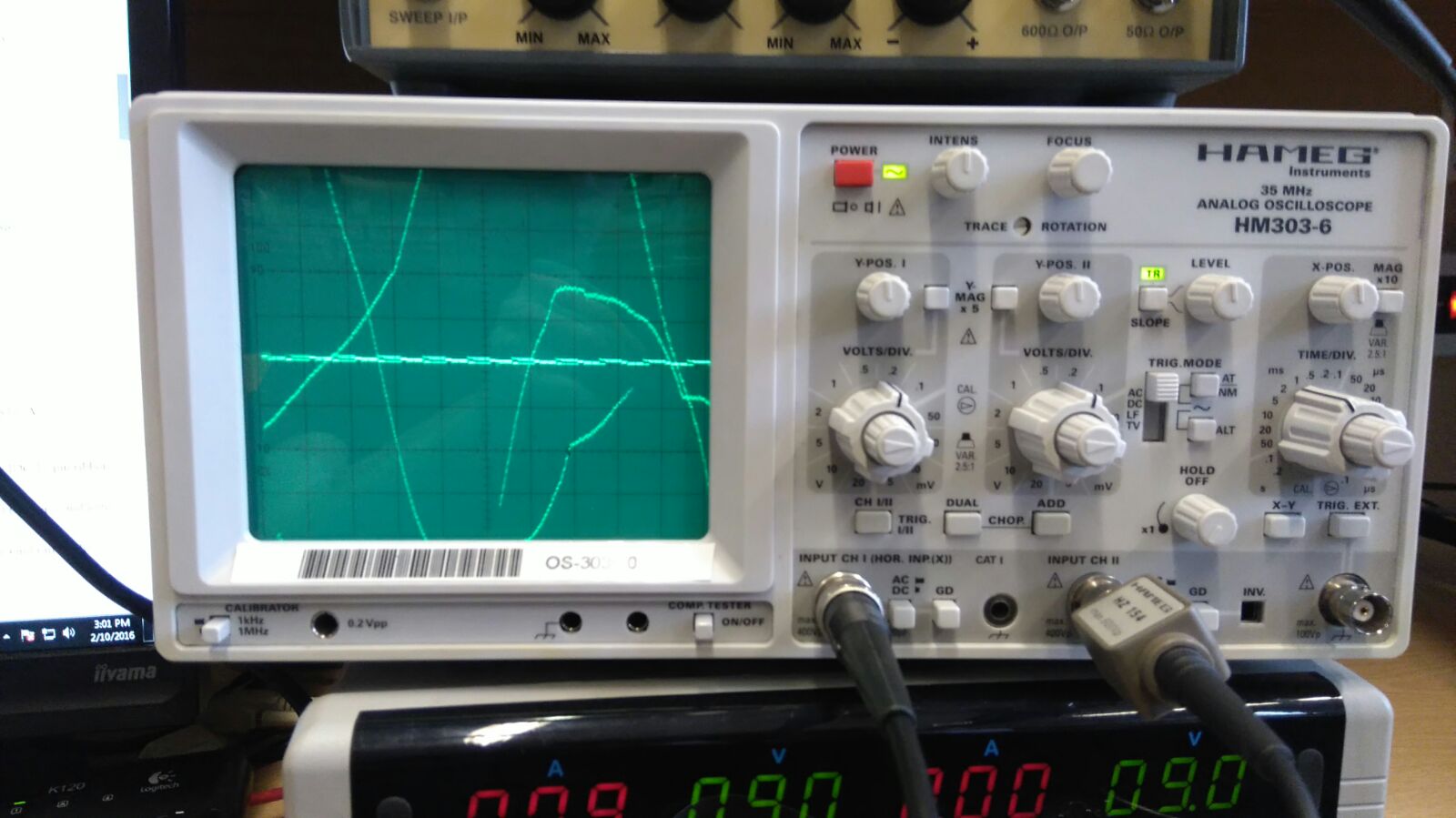
Figure

Q2



Figure

Q3



Figure

Q0 Clear Switch On